WHAT IS CLAIMED IS:

1. An adder circuit comprising:

a first adder cell having:

a first logic gate having a first input that receives a first input signal, a second input that receives a second input signal, and a first output that generates a first logic signal, the first input signal, the second input signal, and the first logic signal each having a logic state, the first logic gate generating the first logic signal in response to the logic states of the first and second input signals, the first logic gate generating an inverted first input signal in response to the first input signal;

a first inverter circuit having a third input that receives a third input signal, a fourth input connected to receive the first logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted first logic signal;

a first carry out circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, and an output; and

a first sum circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, a first sum input connected to the third input signal, a second sum input connected to the inverted third signal, and an output.

2. The adder of claim 1 wherein the carry out circuit includes a first multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state,

and passes a second received signal to the output of the first carry out circuit when the first logic signal has a second logic state.

3. The adder of claim 2 wherein the first received signal is the first input signal.

4. The adder of claim 2 wherein the first received signal is the inverted first input signal.

5. The adder of claim 2 wherein the second received signal is the third input signal.

6. The adder of claim 2 wherein the second received signal is the inverted third signal.

7. The adder of claim 2 wherein the first multiplexer includes:

a first transmission gate having an output connected to the output of the first carry out circuit; and

a second transmission gate having an output connected to the output of the first transmission gate.

8. The adder of claim 2 wherein the first sum circuit includes a second multiplexer that passes a third received signal to the output of the first sum circuit when the logic signal has a first logic state, and passes a fourth received signal to the output of the first sum circuit when the logic signal has a second logic state.

9. The adder of claim 8 wherein the third received signal is the third input signal, an input to the second multiplexer being connected to the first sum input.

10. The adder of claim 8 wherein the third received signal is the inverted third signal.

11. The adder of claim 8 wherein the fourth received signal is the third input signal.

12. The adder of claim 8 wherein the fourth received signal is the inverted third signal.

13. The adder of claim 8 wherein the second multiplexer includes:

a third transmission gate having an output connected to the output of the first sum circuit; and

a fourth transmission gate having an output connected to the output of the third transmission gate.

14. The adder of claim 1 and further comprising a first buffering inverter having an input connected to the output of the first carry out circuit, and an output.

15. The adder of claim 1 wherein the first logic gate is an exclusive OR gate.

16. The adder of claim 1 wherein the first logic gate includes:

a first inverter having a first inverter input connected to the first input of the logic gate, a second inverter input connected to a power node, a third inverter input connected to a ground node, and an output;

a second inverter having a first inverter input connected to the second input of the logic gate, a second inverter input connected to the first input of the logic gate, a third inverter input connected to the output of the first inverter, and an output; and

a transmission gate having a first control input connected to the first input of the logic gate, a second control input connected to the output of the first inverter, a signal input connected to the second input of the logic gate, and an output.

17. The adder circuit of claim 1

wherein the output of the first carry out circuit has a first active state; and

further comprising:

a second adder cell connected to the first adder cell, the second adder cell having:

a second logic gate having a fifth input that receives a fifth input signal, a sixth input that receives a sixth input signal, and a second output that generates a second logic signal, the fifth input signal, the sixth input signal, and the second logic signal each having a logic state, the second logic gate generating the second logic signal in response to the logic states of the fifth and sixth input signals, the second logic gate generating an inverted fifth signal in response to the fifth input signal;

a second inverter circuit having a seventh input that receives a seventh input signal, an eighth input connected to receive the second logic signal, a first output that generates an inverted seventh

signal, and a second output that generates an inverted second logic signal;

a second carry out circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and a second output, the second output of the second carry out circuit having a second active state opposite the first active state; and

a second sum circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and an output.

18. The adder circuit of claim 17and further comprising:

a third adder cell connected to the second adder cell, the third adder cell having:

a third logic gate having an ninth input that receives a ninth input signal, a tenth input that receives a tenth input signal, and a third output that generates a third logic signal, the ninth input signal, the tenth input signal, and the third logic signal each having a logic state, the third logic gate generating the third logic signal in response to the logic states of the ninth and tenth input signals, the third logic gate generating an inverted ninth signal in response to the ninth input signal;

a third inverter circuit having a eleventh input that receives an eleventh input signal, a twelfth input connected to receive the third logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted third logic signal;

a third carry out circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and a second

output, the second output of the third carry out circuit having a second active state; and

a third sum circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and an output.

19. The adder circuit of claim 17 wherein the first adder cell is in a first row and the second adder cell is in a second row.

20. The adder circuit of claim 18 wherein the first adder cell is in a first row, the second adder cell is in a second row, and the third adder cell is in a third row.

21. The adder circuit of claim 14

wherein the output of the first carry out circuit has a first active state; and

further comprising:

a second adder cell connected to the first adder cell, the second adder cell having:

a second logic gate having a fifth input that receives a fifth input signal, a sixth input that receives a sixth input signal, and a second output that generates a second logic signal, the fifth input signal, the sixth input signal, and the second logic signal each having a logic state, the second logic gate generating the second logic signal in response to the logic states of the fifth and sixth input signals, the second logic gate generating an inverted fifth signal in response to the fifth input signal;

a second inverter circuit having a seventh input that receives a seventh input signal, an eighth input connected to receive the

second logic signal, a first output that generates an inverted seventh signal, and a second output that generates an inverted second logic signal;

a second carry out circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and a second output, the second output of the second carry out circuit having a second active state opposite the first active state; and

a second sum circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and an output.

22. The adder circuit of claim 21 and

further comprising a second buffering inverter having an input connected to the output of the second carry out circuit, and an output; and

further comprising:

a third adder cell connected to the second adder cell, the third adder cell having:

a third logic gate having an ninth input that receives a ninth input signal, a tenth input that receives a tenth input signal, and a third output that generates a third logic signal, the ninth input signal, the tenth input signal, and the third logic signal each having a logic state, the third logic gate generating the third logic signal in response to the logic states of the ninth and tenth input signals, the third logic gate generating an inverted ninth signal in response to the ninth input signal;

a third inverter circuit having a eleventh input that receives an eleventh input signal, a twelfth input connected to receive the third

logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted third logic signal;

a third carry out circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and a second output, the second output of the third carry out circuit having a second active state; and

a third sum circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and an output.

23. The circuit of claim 1 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have equivalent signal polarities.

24. The circuit of claim 1 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have different signal polarities.